In the Claims

Please replace all prior versions of claims in the application with the following claims:

1. (Currently amended) A cache memory system, comprising:

an associative cache including a plurality of tag memory locations for storing addresses and a plurality of data memory locations for storing data ~~and addresses associated with the data~~, the memory locations being organized as two or more ways and each address presented to the associative cache being compared with the addresses stored in the tag memory locations in each of the two or more ways; and

at least one controller that enables a first device to access a data memory location in a first way selected from the two or more ways and enables a second device to access a data memory location in a second way selected from the two or more ways, the first device accessing ~~a~~ the data memory location in the first way and the second device being blocked from accessing the first way during access by the first device, the second device accessing ~~a~~ the data memory location in the second way and the first device being blocked from accessing the second way during access by the second device, and the data memory locations in the first and second ways can be accessed concurrently by the first and second devices, respectively.

2.–3. Cancelled

4. (Original) The system of claim 1, in combination with the first and second devices, wherein the first device includes a processor configured and arranged to access the memory locations, and wherein the second device includes a data transfer engine configured and arranged to transfer data between the memory locations and a lower-level memory.

5. (Original) The combination of claim 4, wherein the data transfer engine comprises a DMA controller.

6. (Currently amended) A cache memory system, comprising:

an associative cache including a plurality of tag memory locations to store addresses and a plurality of data memory locations to store data ~~and addresses associated with the data~~, the memory locations being organized as two or more ways and each address presented to the associative cache being compared with the addresses stored in the tag memory locations in each of the two or more ways;

a plurality of cache outputs for providing data retrieved from the data memory locations; and

first and second multiplexers having multiplexer inputs coupled to at least some of the data memory locations and multiplexer outputs coupled to the plurality of cache outputs so as to enable the first multiplexer to select data from a data memory location in a first way selected from the two or more ways and to enable the second multiplexer to select data from a data memory location in a second way selected from the two or more ways, the first multiplexer selecting data from ~~a~~ the data memory location in the first way and the second multiplexer selecting data from ~~a~~ the data memory location in the second way, and the selected data from the data memory locations in the first and second ways being provided concurrently on respective ones of the plurality of cache outputs.

7.-29. (Cancelled)

30. (Currently amended) A method of operating an associative cache having a plurality of tag memory locations for storing addresses and a plurality of data memory locations for storing data ~~and addresses associated with the data~~, the memory locations being organized as two or more ways, the method comprising ~~an act of~~:

(A) accessing with a first device a data memory location in a first way selected from the two or more ways and accessing with a second device a data memory location in a second way selected from the two or more ways, the first device accessing ~~a~~ the data memory location in the first way and the second device being blocked from accessing the first way during access by the first device, the second device accessing ~~a~~ the data memory location in the second way and the first device being blocked from accessing the second way during access by the second device, and the data memory locations in the first and second ways can be accessed concurrently by the first and second devices,

respectively, accessing including comparing each address presented to the associative cache with the addresses stored in the tag memory locations in each of the two or more ways.

31. Cancelled

32. (Original) The method of claim 30, wherein the first device includes a processor, wherein the second device includes a data transfer engine, and wherein the act (A) includes acts of:

(A1) using the processor to access the cache; and

(A2) using the data transfer engine to transfer data between the cache and a lower-level memory.

33. (Original) The method of claim 32, wherein the act (A2) includes an act of:

using a DMA controller to transfer data between the cache and the lower-level memory.

34.–35. Cancelled

36. (Currently amended) A method of operating an associative cache having a plurality of tag memory locations for storing addresses and a plurality of data memory locations for storing data ~~and addresses associated with the data~~, the memory locations being organized as two or more ways, the method comprising an act of:

(A) using multiple decoders to decode respective addresses provided to the cache, including using a first decoder to decode a first address to access a data memory location in a first way selected from the two or more ways and using a second decoder to decode a second address to access a data memory location in a second way selected from the two or more ways, the first address accessing ~~a~~ the data memory location in the first way and the second address accessing ~~a~~ the data memory location in the second way and the data memory locations in the first and second ways can be accessed concurrently by the first and second addresses, respectively, further comprising comparing each address presented to the associative cache with the addresses stored in the tag memory locations in each of the two or more ways.

37.-38 Cancelled

39. (Previously presented) The method of claim 36, wherein each of the multiple decoders is preceded by a multiplexer that receives the first and second addresses as inputs and provides a selected one of the first and second addresses as an output to the decoder it precedes, and wherein the method further comprises an act of:

(B) controlling at least one of the multiplexers to select one of the first and second addresses as its output while concurrently controlling another of the multiplexers to select the other of the first and second addresses as its output.

40. Cancelled

41. (Currently amended) A cache memory system, comprising:

an associative cache including a plurality of tag memory locations for storing addresses and a plurality of data memory locations for storing data ~~and addresses associated with the data~~, the memory locations being organized as two or more ways and each address presented to the associative cache being compared with the addresses stored in the tag memory locations in each of the two or more ways; and

means for enabling a first device to access a data memory location in a first way selected from the two or more ways and enabling a second device to access a data memory location in a second way selected from the two or more ways, the first device accessing ~~a~~ the data memory location in the first way and the second device being blocked from accessing the first way during access by the first device, the second device accessing ~~a~~ the data memory location in the second way and the first device being blocked from accessing the second way during access by the second device, and the data memory locations in the first and second ways can be accessed concurrently by the first and second devices, respectively.

42.-45. Cancelled